# A Fully-Bypassed 6-Issue Integer Datapath and Register File on an Itanium™ Microprocessor

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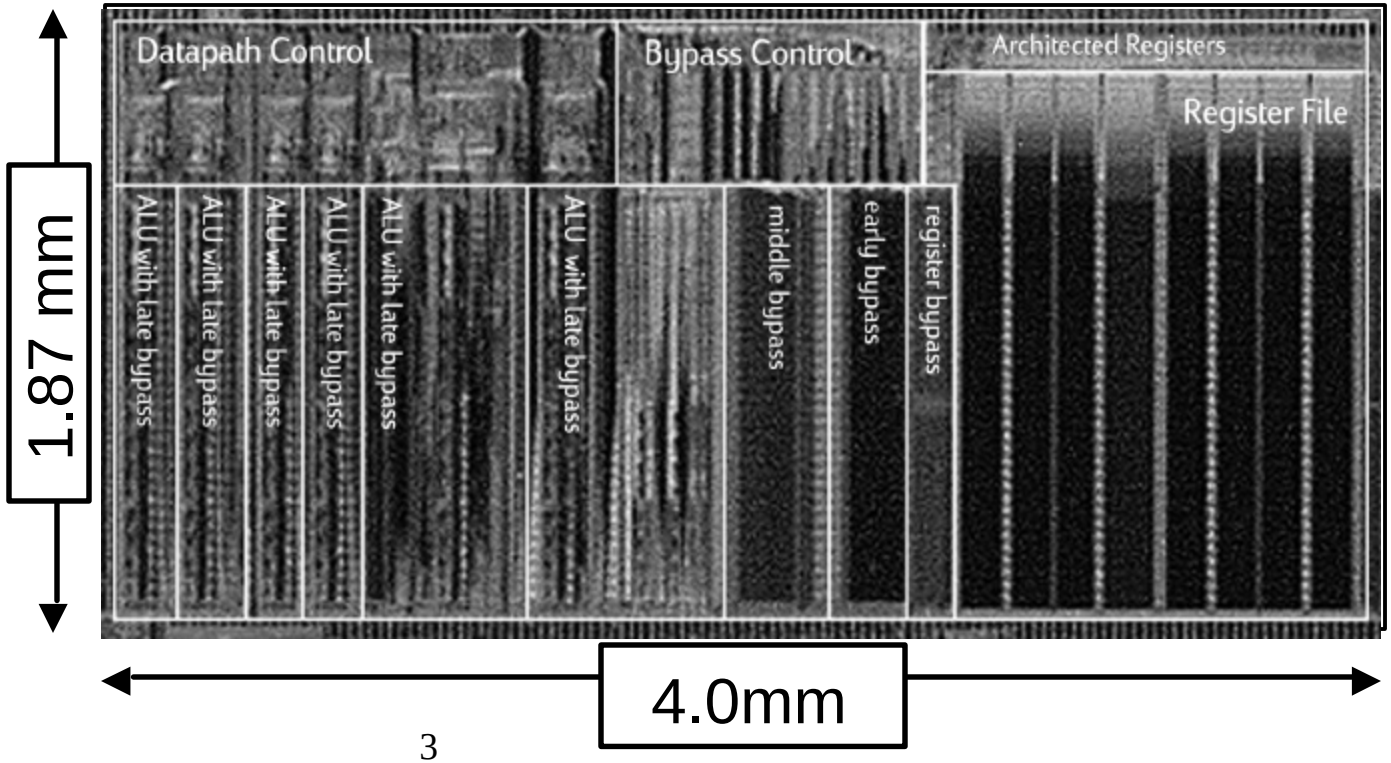
# Presentation Overview

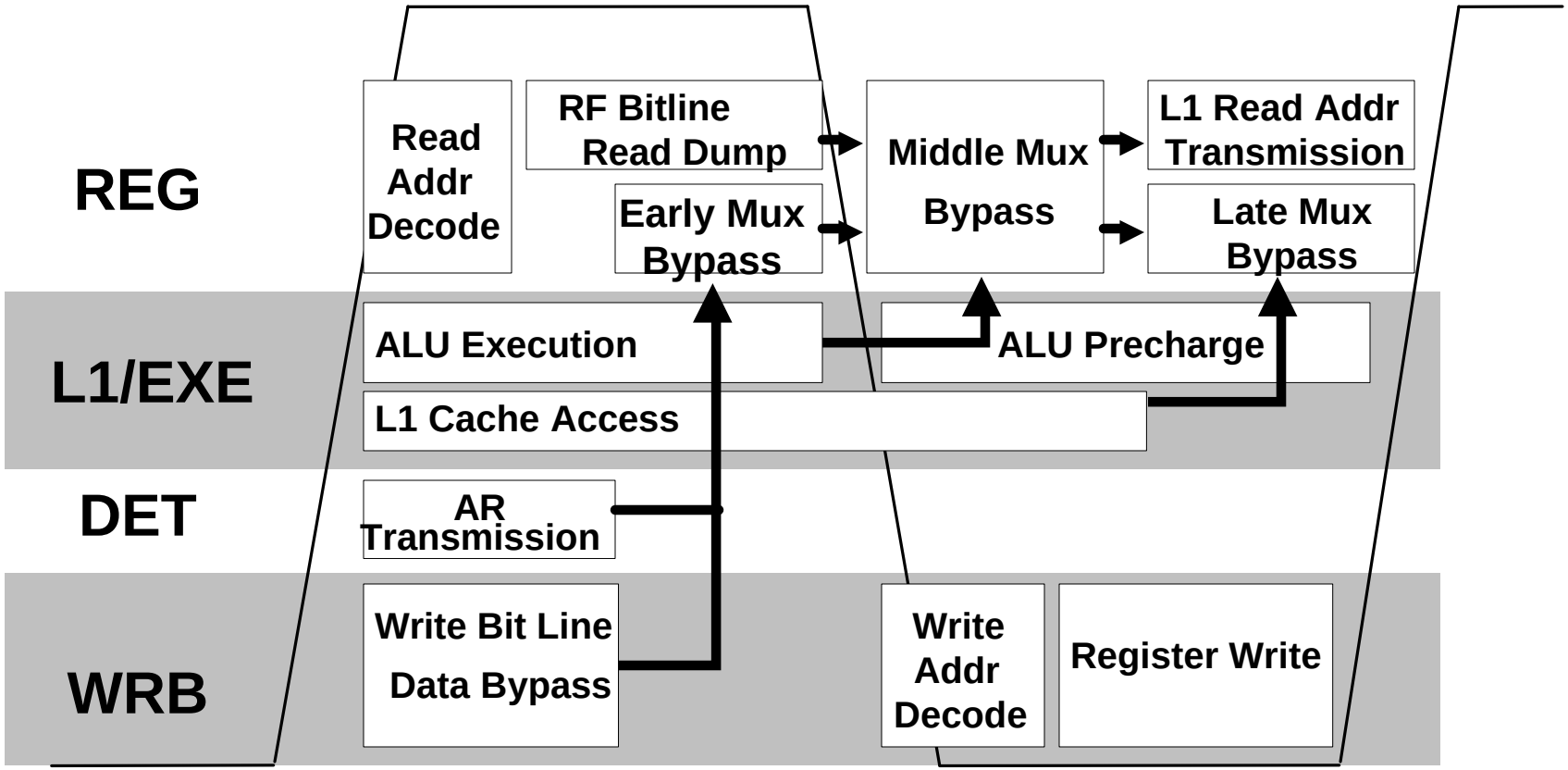
- Integer Datapath (IEU) Features and Timing
- Register File Operation
- Operand bypassing
- ALU result generation

# IEU Features

- 128 x 64 bit 20 ported general registers (16 banked)
- 6 symetrically bypassed 64 bit ALUs, 1 shifter
- 4 stage bypass with 34 sources and 16 destinations
- 2 read and 2 write L1D cache ports
- IA 32 instruction support



# IEU Timing

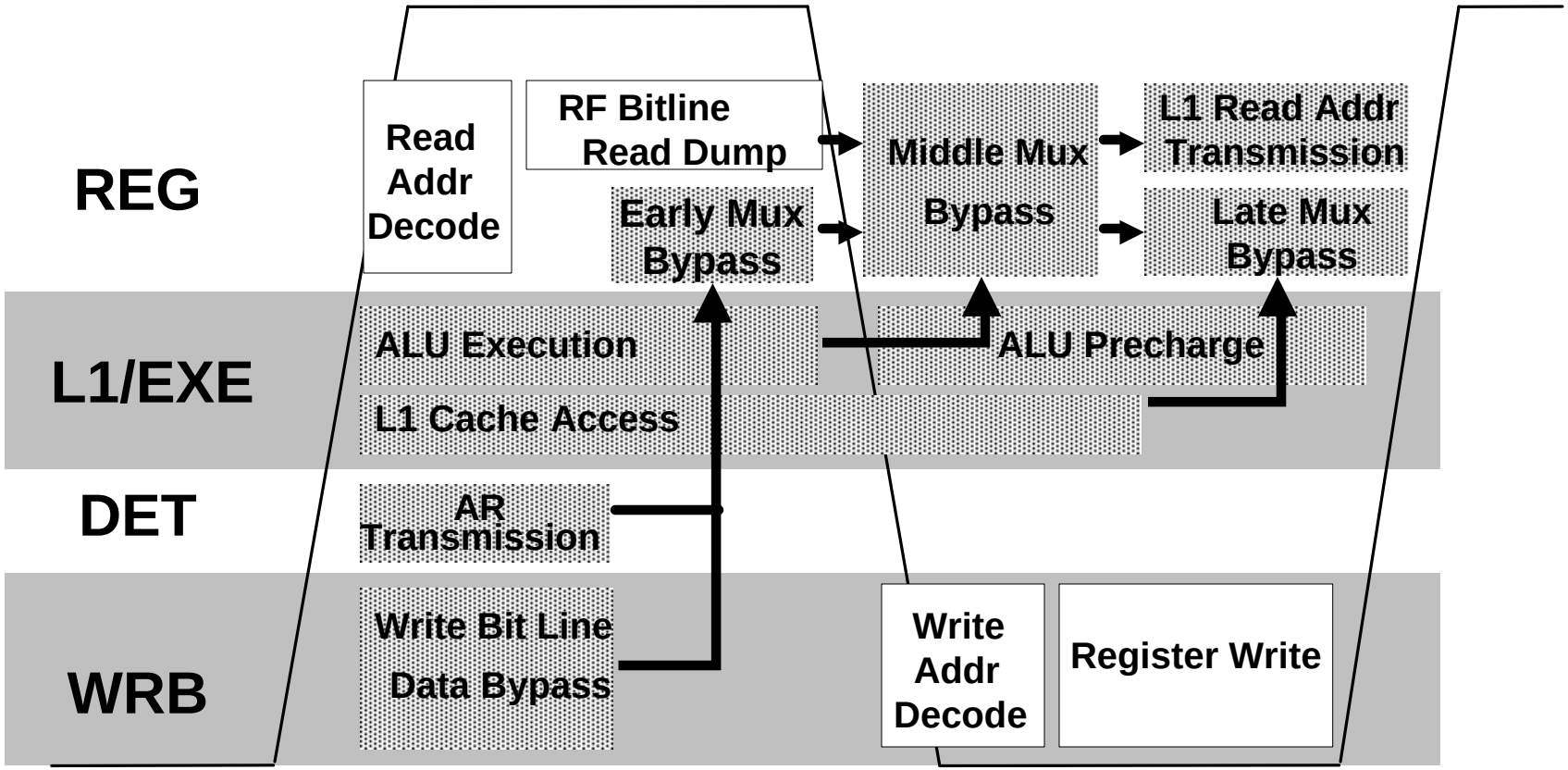

REG
L1/EXE
DET
WRB
Read Addr Decode
RF Bitline Read Dump
Early Mux Bypass
Middle Mux Bypass
L1 Read Addr Transmission
Late Mux Bypass
ALU Execution
ALU Precharge
L1 Cache Access
AR Transmission
Write Bit Line Data Bypass
Write Addr Decode
Register Write

# Register File Features/Overview

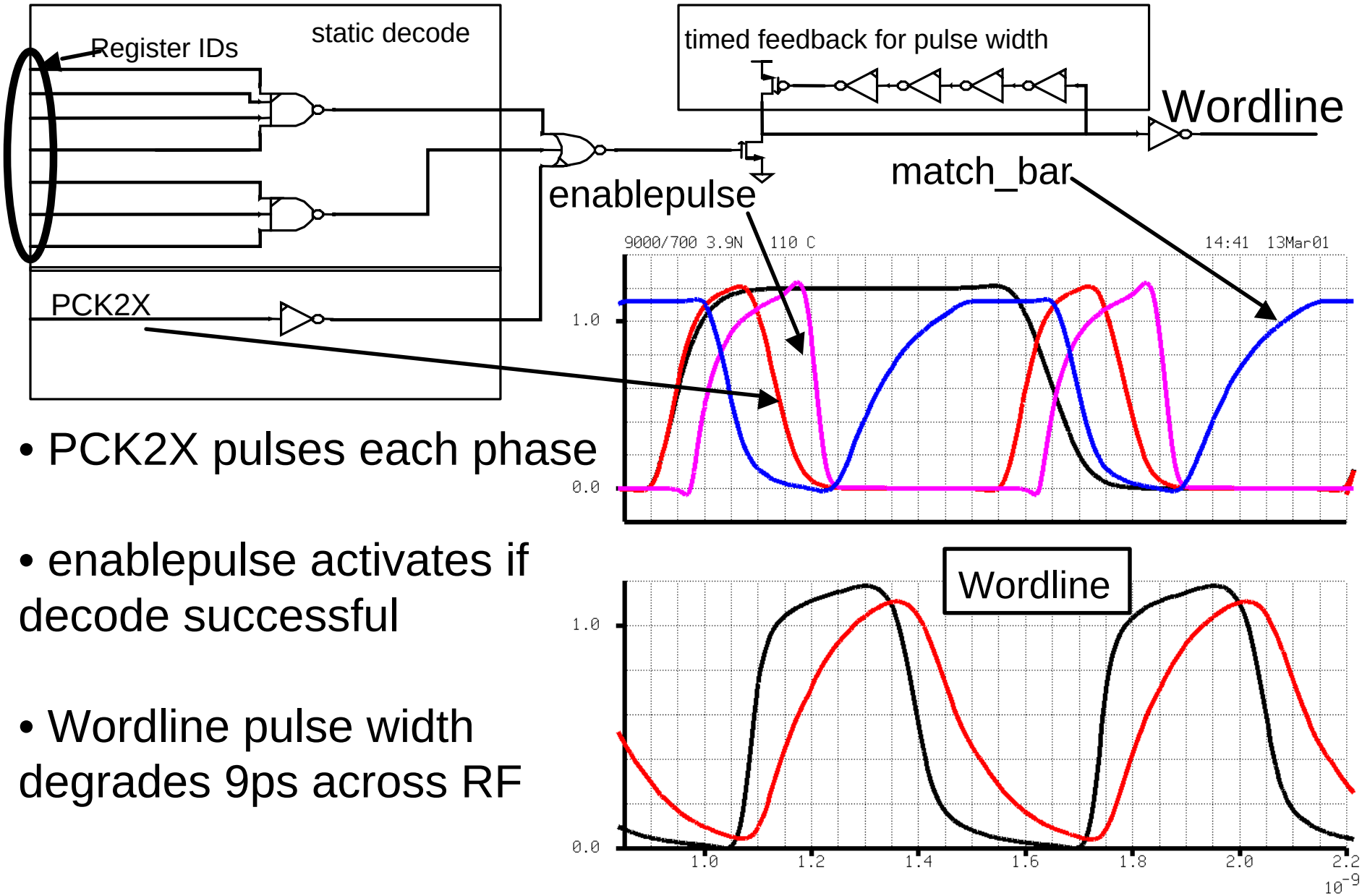
| | |
|---|---|
| Frequency (GHz) | 1.0 |
| Write Ports | 8 |
| Read Ports | 12 |
| Registers | 128 64bit |
| Write Type | Single Ended |
| Read Type | Single Ended |
| Array Area | 1.67mm$^2$ |
| Decoder Area | 0.39mm$^2$ |
| Global Overhead | 0.13mm$^2$ |
| Total Size | 2.2mm$^2$ |

- 8 of 12 Read Decoders are reused for writes saving 8 decoders per register
- Wordlines are pulsed allowing one wordline to be used for both read and write
- Antimiller devices are used to reduce coupling on dynamic output nodes
- Write bitlines are used to bypass multimedia unit data to the integer datapath on the non-write phase.

# IEU Timing – Register File

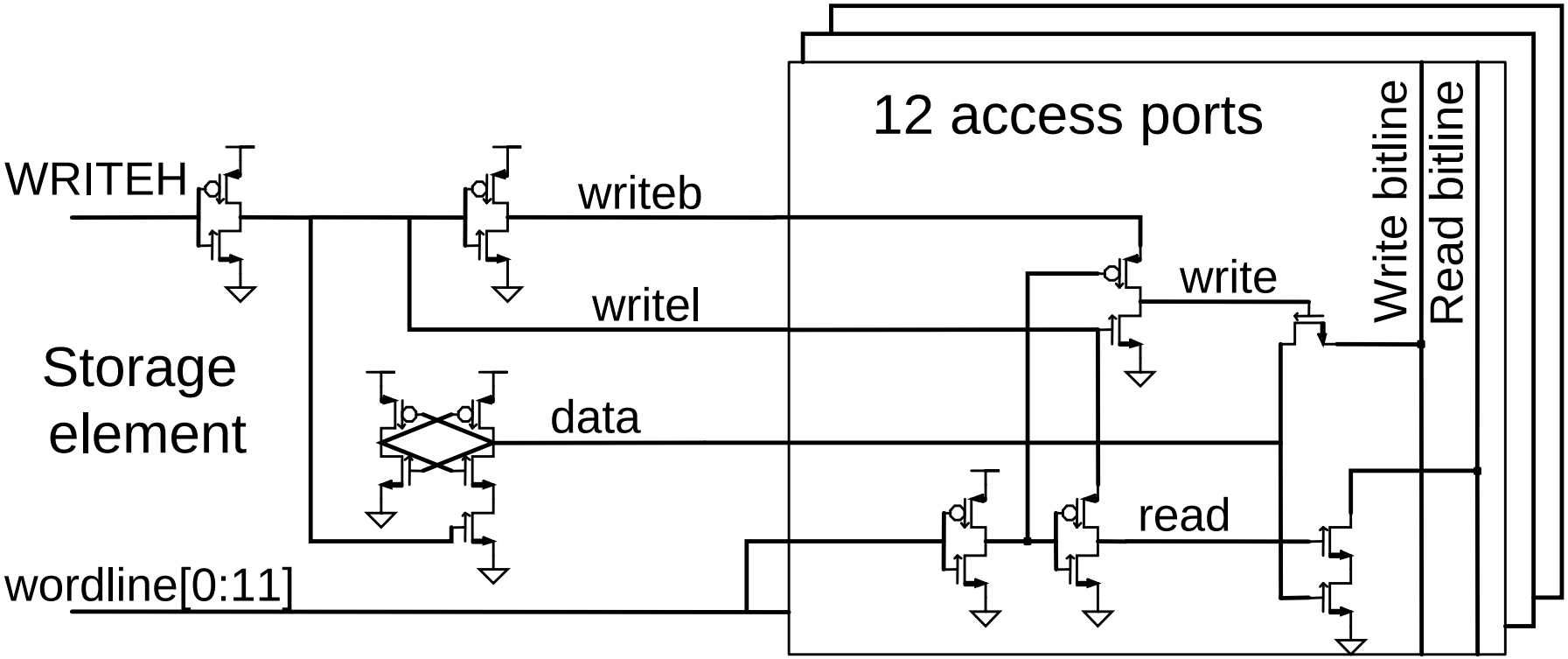


# Register File Decode




- PCK2X pulses each phase
- enablepulse activates if decode successful
- Wordline pulse width degrades 9ps across RF

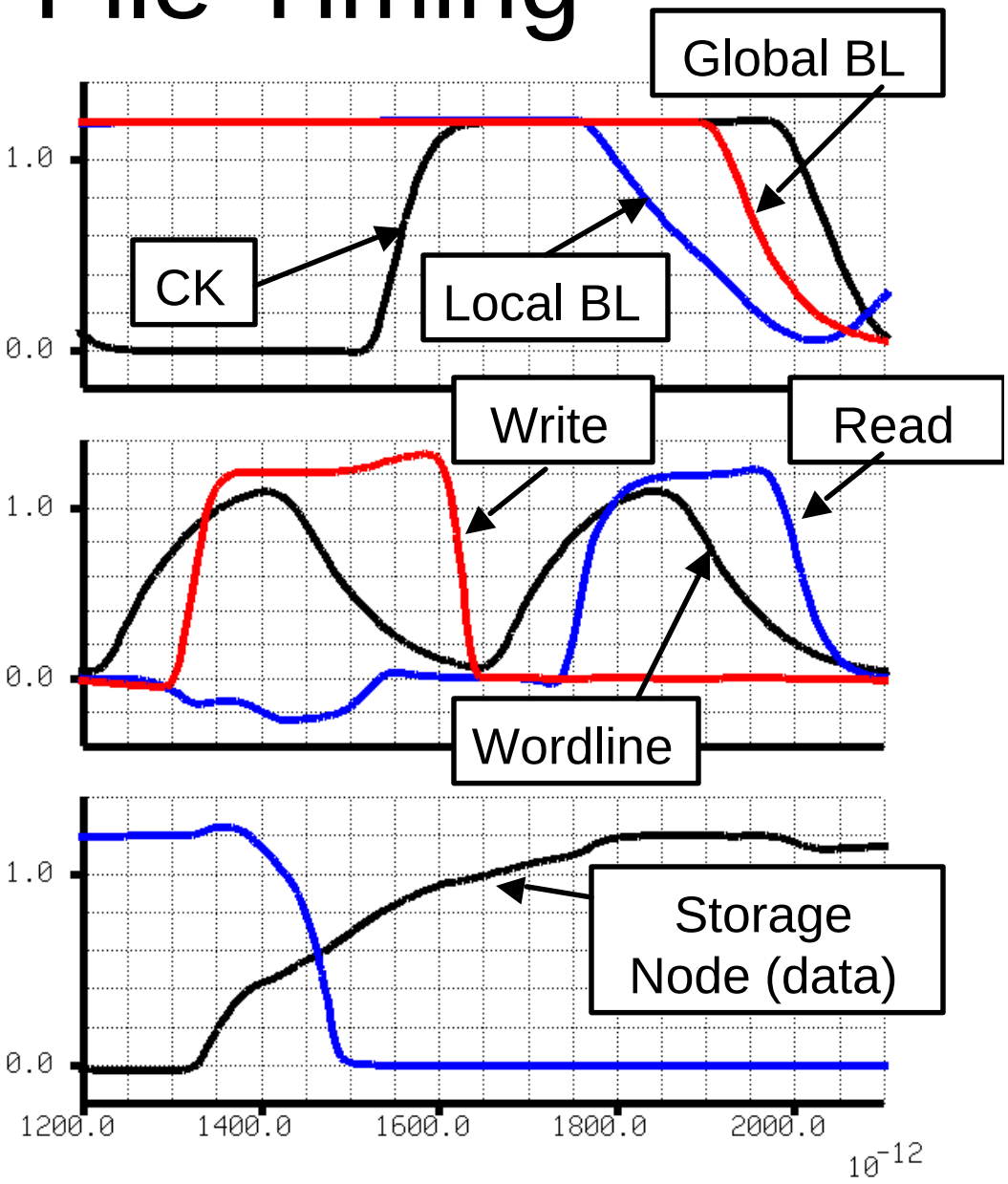
# Register File Storage Cell




- Storage Cell is tristated to allow for NFET only writes
- Each access port has discriminating wordline buffer to protect from wordline noise and establish read or write

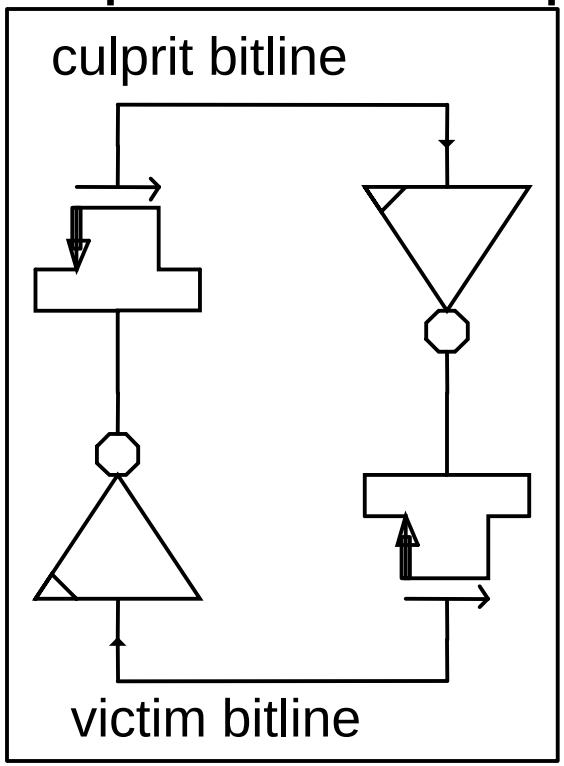
# Register File Timing

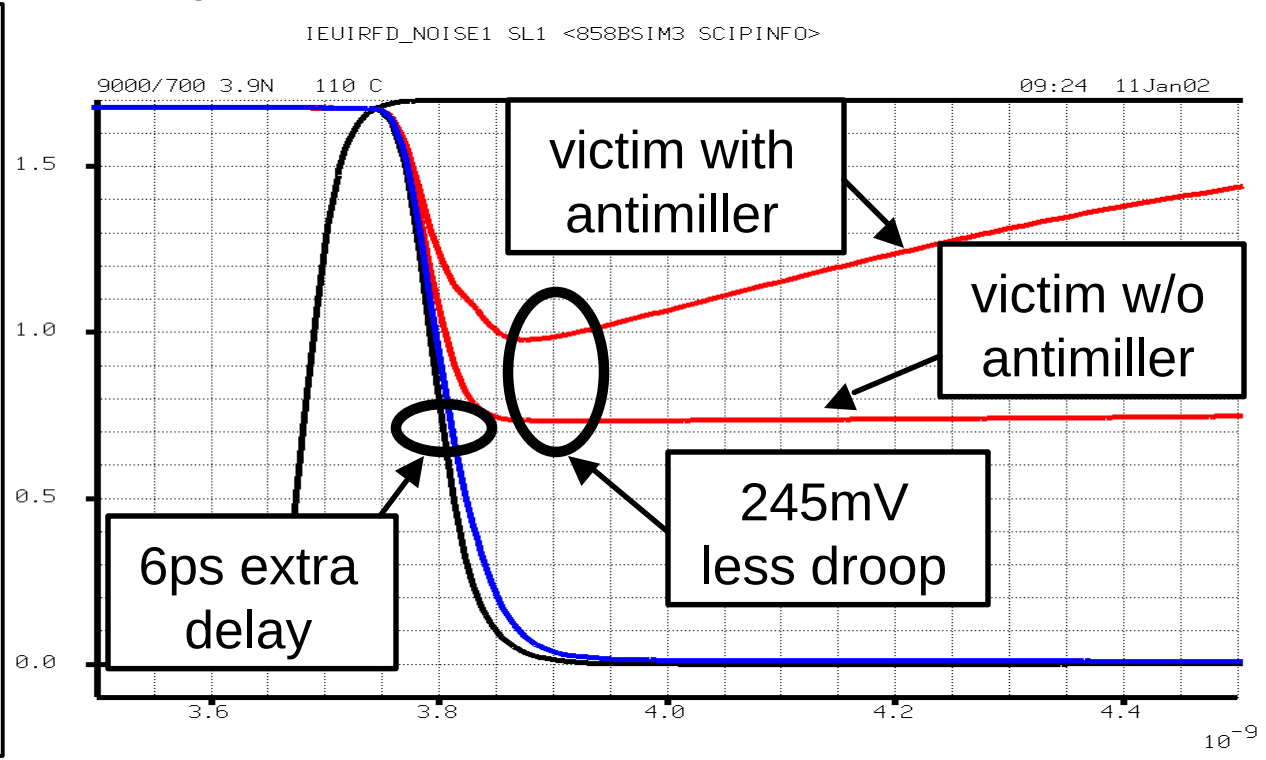
- A 2 level hierarchical bitline is employed
- Local read/write signals generated from each wordline
- Storage node
  - 80% VDD end of write
  - 100% VDD at read



# Register File Noise Solutions

- Toplevel register read bitlines: 2mm, min space, precharge-pulldown, metal 4
- Antimiller devices reduce crosstalk induced droops
- Noise margins improved significantly with a small performance penalty



# Bypass Overview

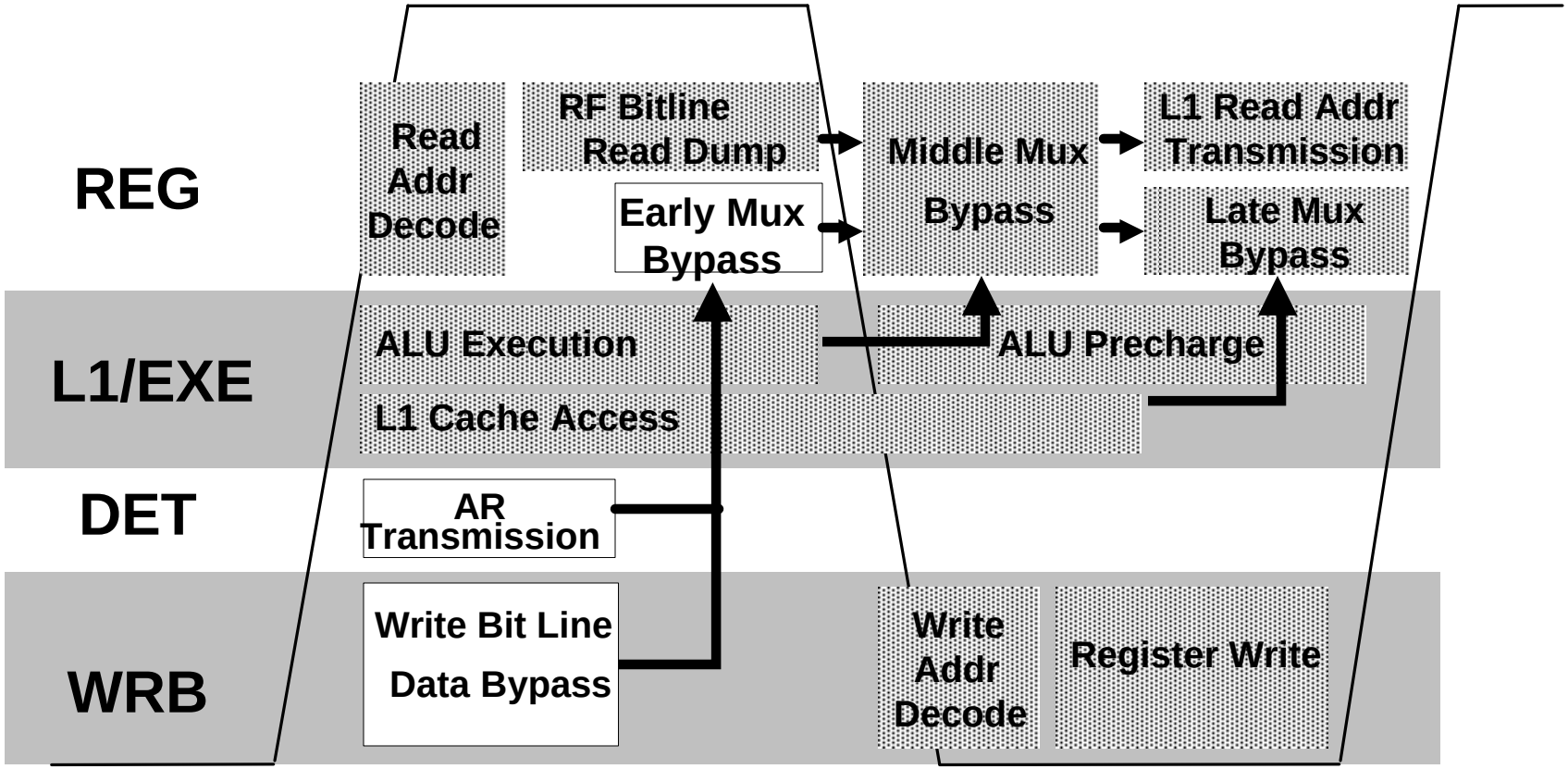
- Bypass has four stages

| Mux | Ratio | Inputs | Circuit Type |
|---|---|---|---|
| RFB | 2:1 | IEU + MMU WRB | Pulse Predischarge |
| Early | 16:1 | RFB + IEU DET | Phase 1 Dynamic |
| Middle | 8:1 | ALU + RF read +Early | Phase 2 Dynamic |
| Late | 4:1 | L1D + Middle + opcode | Pseudo-Dynamic |

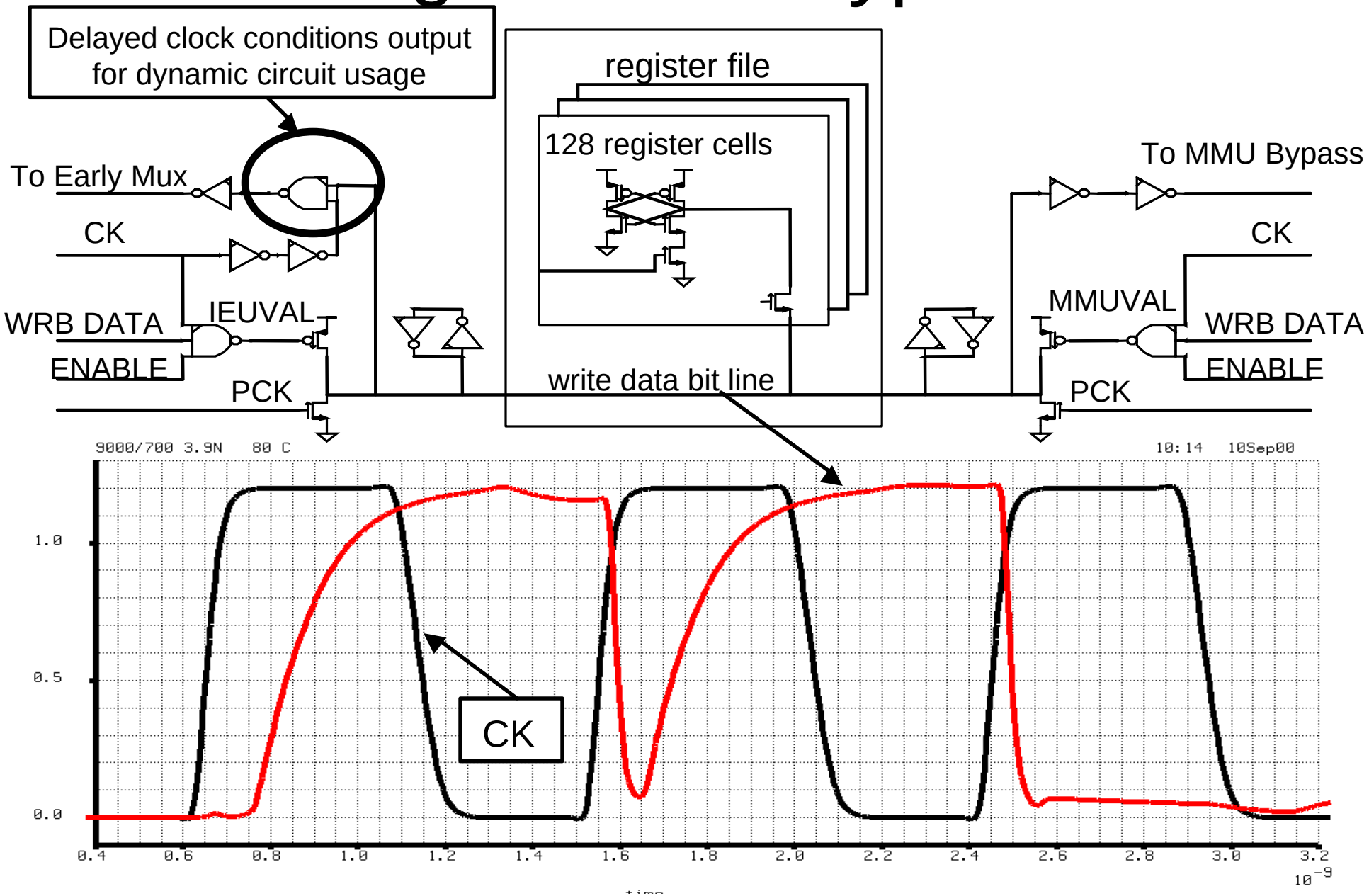
- Register File Bypass (RFB) and Early Bypass occur in parallel with register reads and ALU operation

- Bypass order optimizes data and control availability and architectual priority

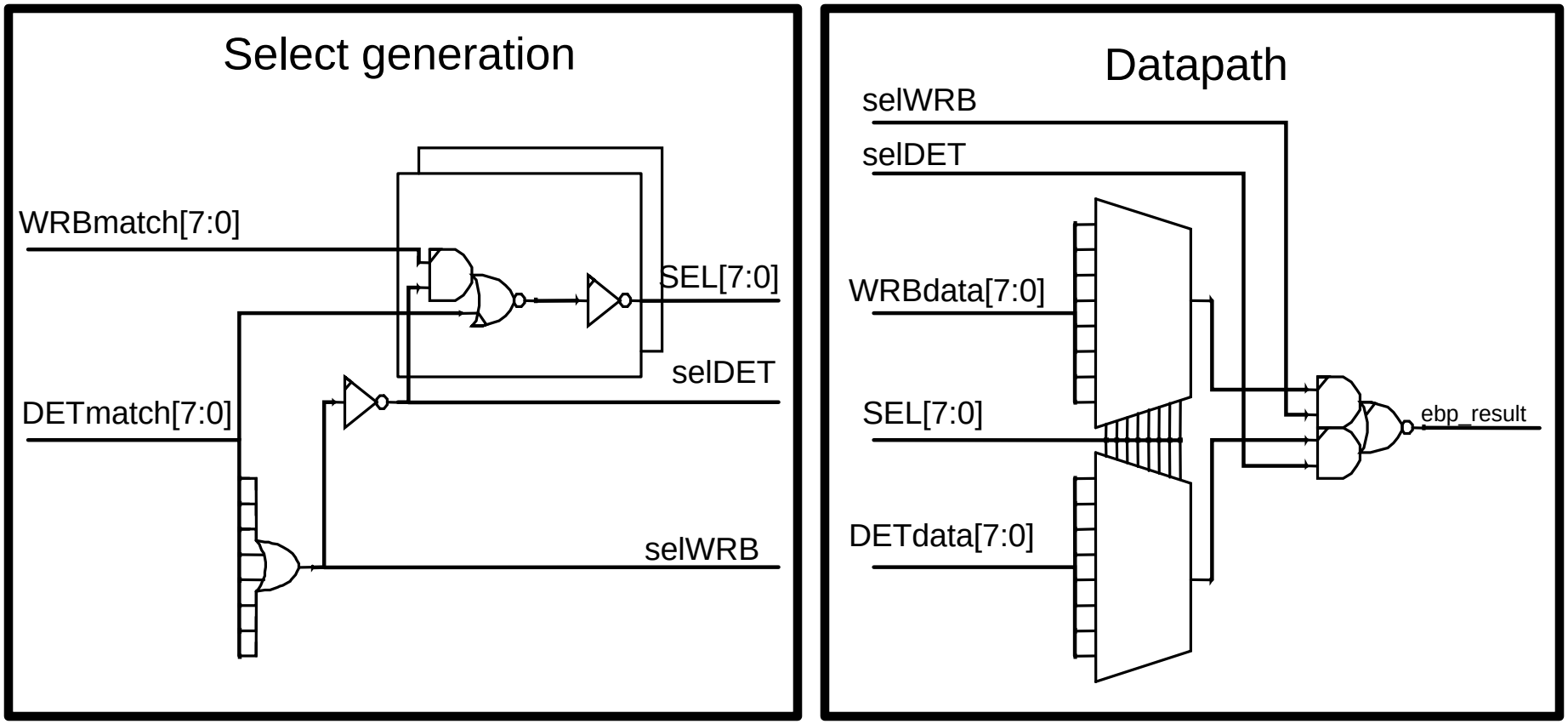
# IEU Timing – Phase 1 Bypass



# Register File Bypass

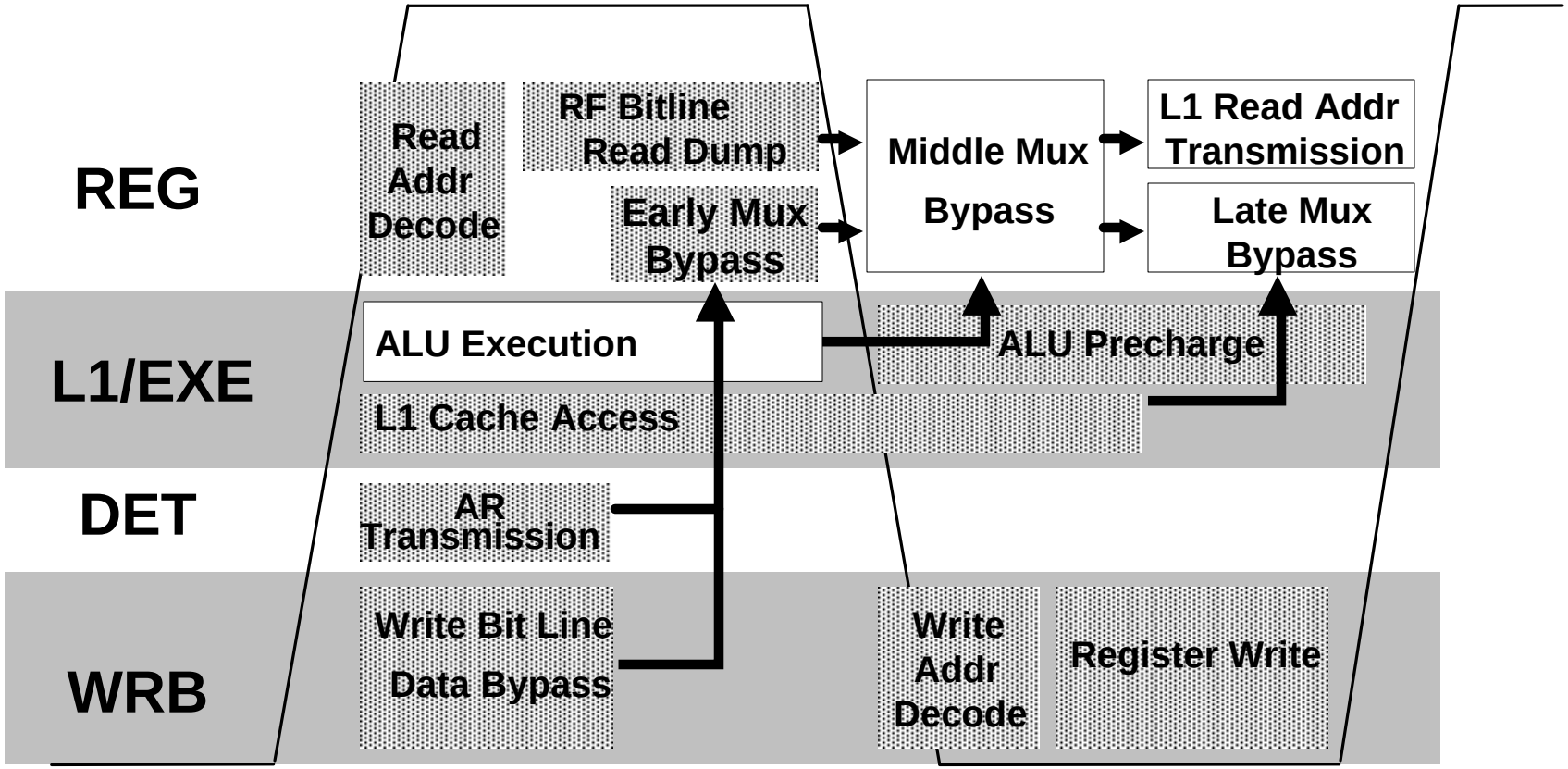


# Early Bypass

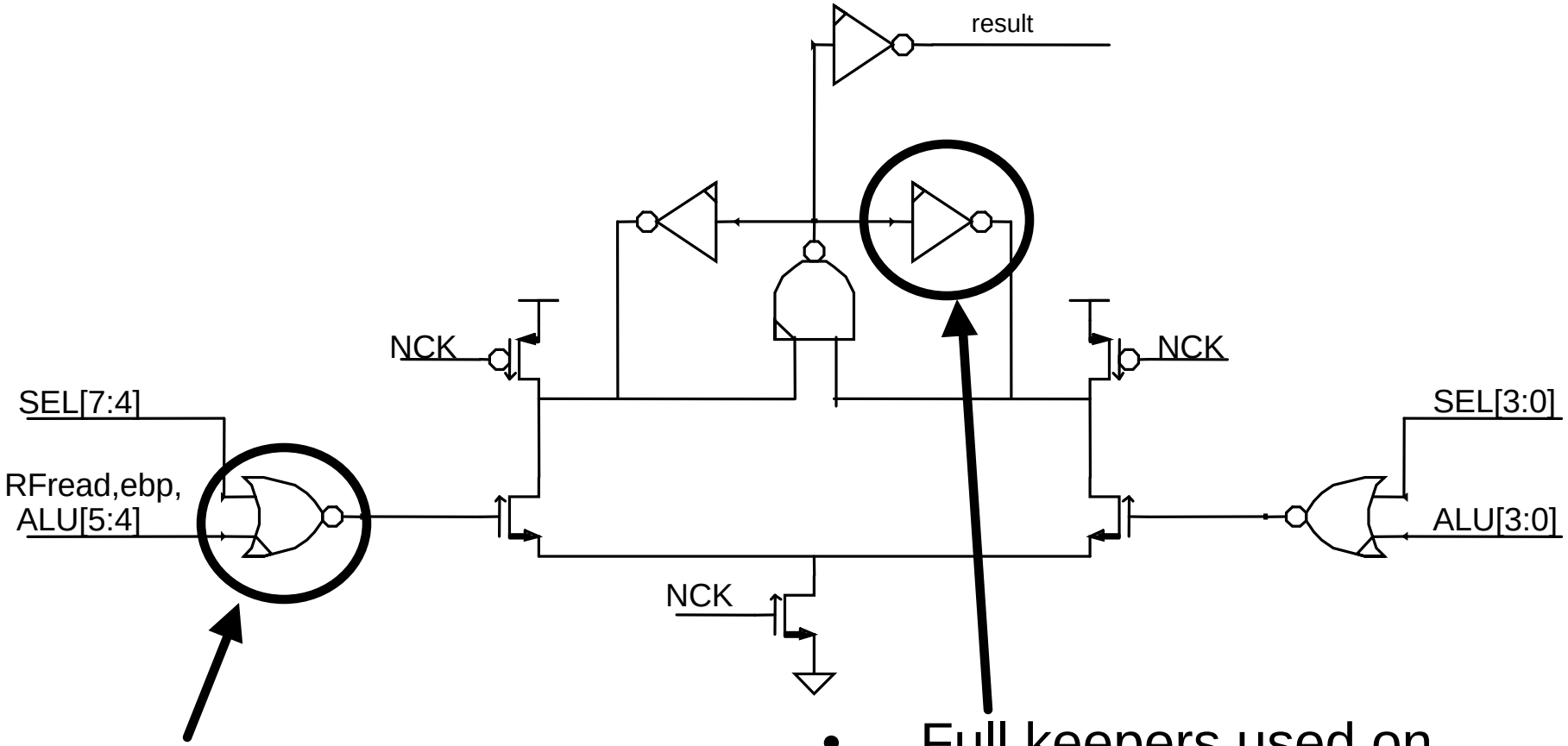



- 16 Comparator outputs (WRBmatch/DETmatch) are reduced to 10 selects saving 96 wires
- Data inputs are conditioned with CK to remove clock pulldown FET from domino stack

# IEU Timing – Phase 2 Bypass & Results

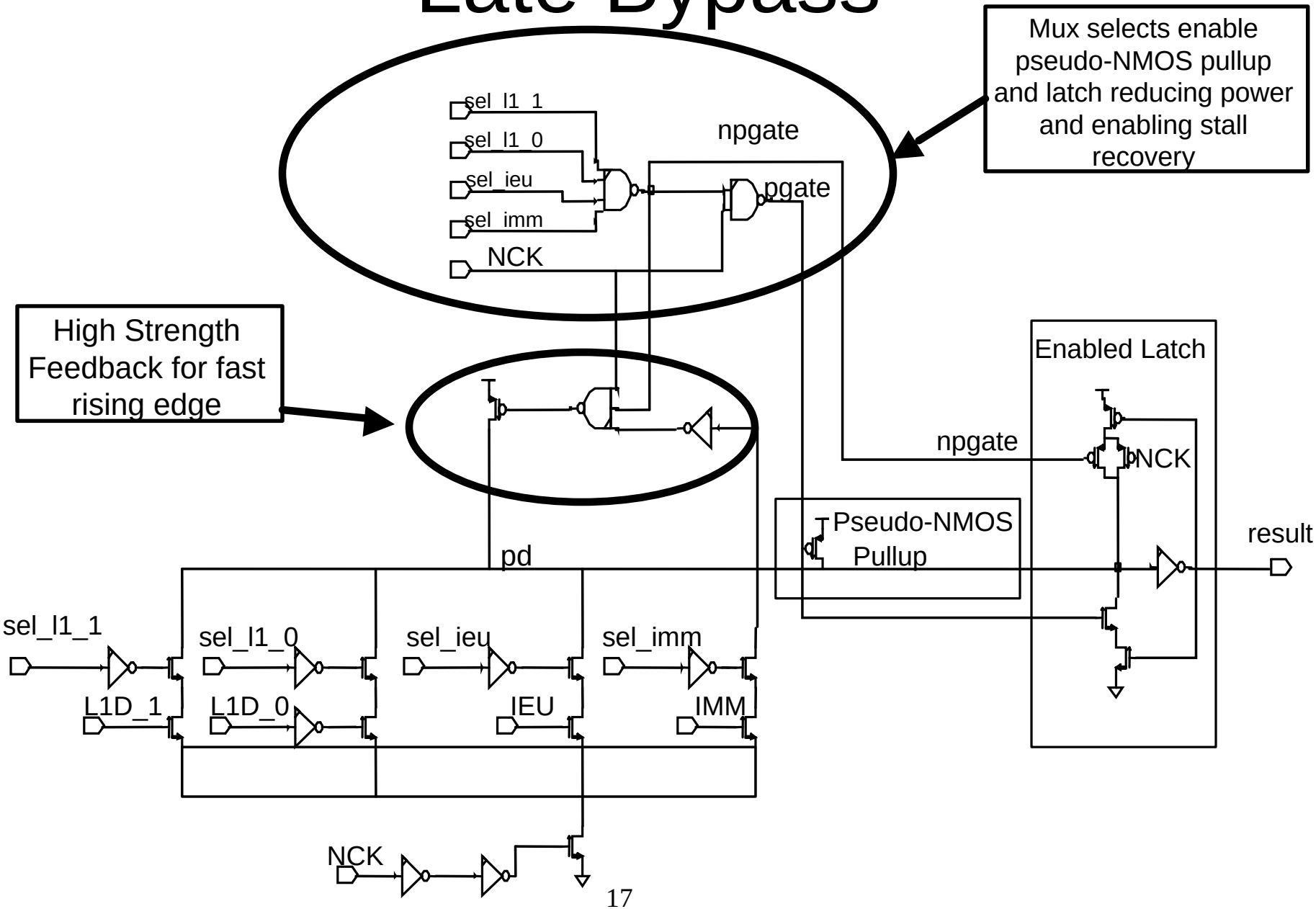


# Middle Bypass

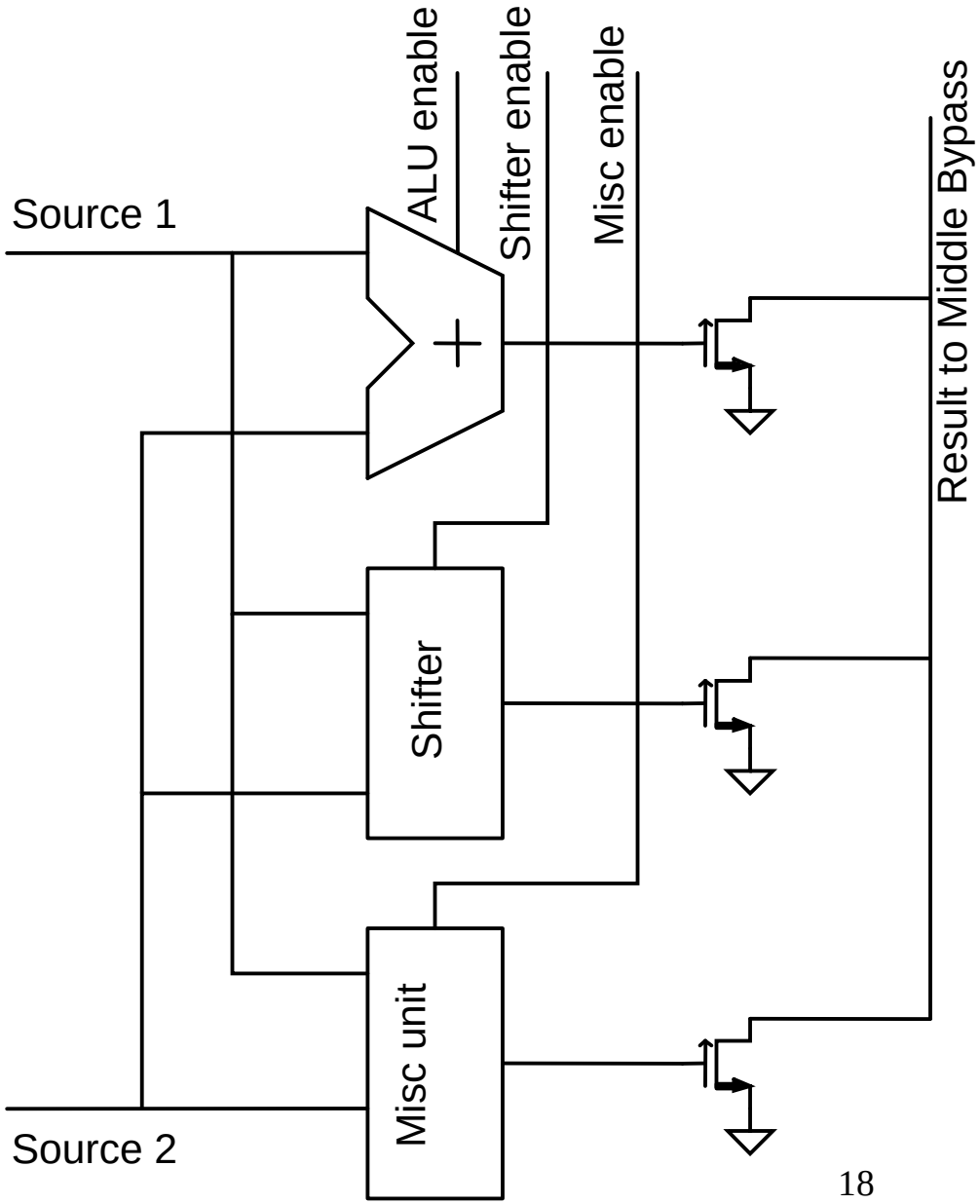



- Active low inputs and static receivers reduce impact of noise
- Full keepers used on dynamic nodes to allow phase 1 (CK) inputs to be “caught” removing the need for a latch

# Late Bypass


Mux selects enable pseudo-NMOS pullup and latch reducing power and enabling stall recovery
sel_l1_1
sel_l1_0
sel_ieu
sel_imm
NCK
npgate
pgate
High Strength Feedback for fast rising edge
Enabled Latch
npgate
NCK
Pseudo-NMOS Pullup
result
pd
sel_l1_1
sel_l1_0
sel_ieu
sel_imm
L1D_1
L1D_0
IEU
IMM
NCK

# Results Datapath




- Functional units (FU) are pre-enabled saving power and removing the need for a result mux
- FU outputs flow transparently through the middle and late bypasses stopping only for the CK clock boundry at the input to the FU
- Antimillers are used to enable long precharge pulldown results busses

# Summary

- A 7.48mm$^2$ integer datapath is constructed with 128 general registers,6 fully bypassed ALUs and 4 cache address ports using:
  - Aggressive register file techniques delivered high performance/bandwidth in a small foot print
  - Active low signaling and antimiller circuitry make long precharge-pulldown nets feasible
  - Pre-enabled functional units reduce power consumption 15% and remove logic stages from bypass network
  - Pulse circuits in register file and bypass to deliver high performance while remaining area efficient